Noise Analysis of Pixel-Parallel ADC

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***Abstract*— This study discusses the noise of a pixel-parallel ADC. An image sensor using a pixel-parallel ADC was designed to operate on subthreshold current, usually less than 1 µA per pixel, constrained by the increase in the number of simultaneous operations of the comparator. Therefore, the mechanism of noise generation in this imager is dominated not by saturation but by diffusion current. We analyzed the design parameters having sensitivity to noise through a circuit model equation. The analysis and prototype measurement results were applied to the transient noise simulation performed using 90 nm-pixel/40 nm-logic model parameters. It was found that the effective design parameters are the operation current of the comparator, slope of the DAC, and load capacitance of the 2nd node. Finally, leveraging the feedback from this study, we designed a chip with stacked 25.2 Mpixels of 5.94 µm², achieving 167 μV_{rms} at 0 dB analog gain and 120 fps operation with a power consumption of 1545 mW at 14 bit resolution.**

Keywords—pixel-parallel ADC, random noise, digital pixel sensor, CMOS image sensor, subthreshold, single-slope

I. Introduction (*Why pixel-parallel ADC?*)

From the early 2000s, column-parallel ADCs have been widely used because of their speed and narrow noise bandwidth. Various ADCs (cyclic pipeline [1], cyclic [2], SAR [3], DT-ΔΣ [4], CT-ΔΣ [5], single-slope [6][7], adaptive single-slope [8]) were researched. The basic hypotheses were as follows:

operating multiple slow ADCs in parallel results in a better performance than that of a single ADC operating at a video rate.

Currently, the widely used single-slope(SS)-ADC allows digital CDS. It has the advantages of a simple circuit configuration and small area. Furthermore, it effectively uses the floating diffusion (FD) in a pixel as a signal sample-and-hold (S/H) circuit, which is indispensable in ADC. This S/H circuit is referred to as "complete transfer" in the field of image sensor engineering. Similarly, the sampling transistor is named as “transfer gate.” Circuit design engineers can consider this as “a one-time kT/C-less S/H circuit.” Designing a S/H capacitance as small as possible was revolutionary because the pixel signal could be amplified by the capacitance ratio of the PD and FD in the voltage domain without increasing kT/C noise. Furthermore, SS-ADCs exhibit high performance for noise cancellation (fixed pattern and random noise) of the SS-ADC itself, which also serves as an analog CDS circuit through a digital CDS.

Pixel-parallel ADCs [9][10] are expected to achieve a better performance than column-parallel ADCs. The hypotheses were as follows:

operating even slower ADCs in a massively parallel manner results in better performance.

In 2018, a prototype in-pixel SS-ADC with a stacked structure based on a pixel-wise Cu-Cu connection [11] proved this hypothesis by attaining the best figure of merit (FoM) reported to date. In in-pixel circuit implementations, inevitable constraints exist on circuit area and power consumption with respect to column-parallel ADCs operating on a saturation current. Pixel-parallel ADCs must operate at subthreshold currents. An analysis of the design parameters that have an impact on noise in this current region was conducted in the past [12]; however, the circuit configuration was different. Transient-based AC noise simulations [13], [14] have shown that the load capacitor is a sensitive parameter. However, a 100 fF in-pixel capacitor for noise reduction may not be cost-effective for pixel-parallel ADCs that do not exploit expensive special processes, such as DRAM.

In this study, we extracted sensitive design parameters from the experimental results of the prototype, equivalent circuit model calculations, and transient noise simulations. Table 1 summarizes the parameters used in the formulas employed in this study.

II. Measurement Results and Dominant Noise

As shown in Figure 1, the evaluation results of the prototype [11] revealed that no drastic change in noise occurred, even when the CDS interval was extended. It was found that this significantly depended on the analog gain adjusted through the DAC slope; it was not dominated by dark-current shot noise and flicker (1/f) noise. According to other studies [15], the carrier trap at low V_{gs} voltage has the effect of increasing time-to-capture (τ_C) and decreasing 1/f noise. Thus, in the subthreshold current region, carriers are difficult to trap in defects once de-trapping occurs. Furthermore, the FD dark-current shot noise was not dominant in this prototype, and could be better designed for subsequent device fabrication.

Table 1: Parameters of Calculation Formulas

Parameter	Dimension	Comment
k	JK^-1	Boltzmann constant, 1.38 ×10^-23
T	K	Temperature
Ids	A	Transistor operation current (Half of comparator operation current)
q	C	Elementary charge
γn	dimensionless	Noise factor 1~2/3
γp	dimensionless	Noise factor 1~2/3
κn	dimensionless	NMOS Body effect (∂Ψs/∂Vg), where Ψs is the surface potential
κp	dimensionless	PMOS Body effect (∂Ψs/∂Vg)
Kramp	V/s	Slope of DAC
Co	F	Load capacitance
V_{TH}	V	Threshod voltage of comparator
λ	1/V	Channel length modulation, (=Inverse of early voltage)

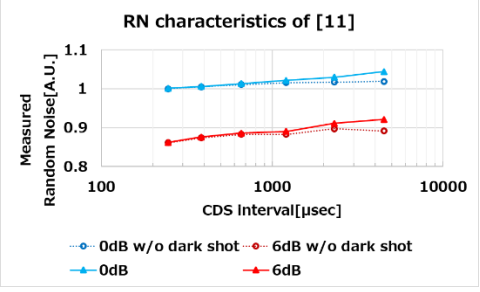

Figure 1: Measured random noise as a function of CDS interval.

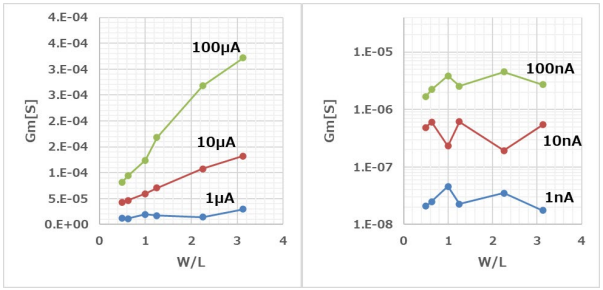

Figure 2: Transconductance for each W/L ratio under a parameter of current ranging from 100 μA to 1 nA.

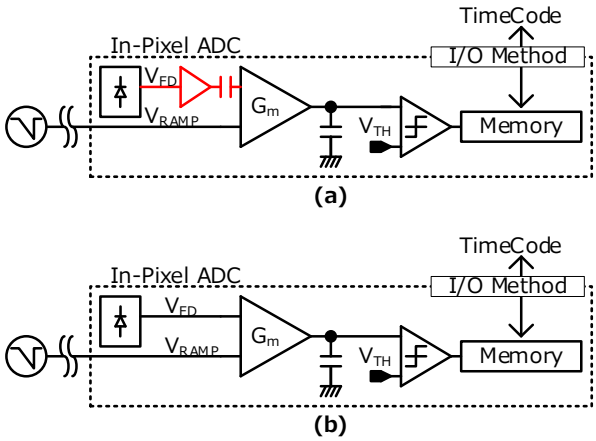

Figure 3: (a) Simplified structure of pixel-parallel ADC [16],[17]; (b) pixel-parallel ADC [11] without implementing a source follower or sample-track capacitor (this study).

Figure 2 shows the measured transconductance of the transistors under each current condition. The transconductance in the subthreshold current region (less than 1 μA) does not depend on the W/L ratio of the transistor. This result implies that it is difficult to control the thermal noise power spectrum density (PSD) through the adjustment of the W/L ratio. Therefore, the noise reduction strategy of pixel-parallel ADCs results in the design of a suitable noise bandwidth.

III. Noise Analysis

As shown in Figure 3, the source follower and DC-cut sample-and-track capacitors, which are implemented in conventional column-parallel and other pixel-parallel ADCs [16],[17], are not implemented in the proposed pixel ADC structure. The FD is directly connected to the comparator (CM). Therefore, the dominant noise source in the proposed pixel-parallel ADC is the thermal noise of the CM.

A. Small-signal analysis

Considering the current flow of Figure 4, we can obtain

$$(\boldsymbol{V_{dd}-V_{mir}})\boldsymbol{g_{mp}}=(\boldsymbol{V_{RAMP}-V_{com}})\boldsymbol{g_{mn}}+(\boldsymbol{V_{mir}-V_{com}})/\boldsymbol{r_{on}}$$

$$(\boldsymbol{V_{dd}-V_{mir}})\boldsymbol{g_{mp}}+(\boldsymbol{V_{dd}-V_{out}})\boldsymbol{r_{op}} = \boldsymbol{I_{out}}+(\boldsymbol{V_{FD}-V_{com}})\boldsymbol{g_{mn}} + (\boldsymbol{V_{out}-V_{com}})/\boldsymbol{r_{on}}$$

Assuming $g_m \cdot r_o \gg 1$, we can approximate $g_m + \frac{1}{r_o} \fallingdotseq g_m$

$$\boldsymbol{I_{out}}=\boldsymbol{V_{RAMP}}\cdot\boldsymbol{g_{mn}}-\boldsymbol{V_{out}}\left(\frac{\boldsymbol{1}}{\boldsymbol{r_{on}}}+\frac{\boldsymbol{1}}{\boldsymbol{r_{op}}}+\boldsymbol{\beta}\cdot\boldsymbol{g_{mn}}\right) \quad (1)$$

Here, $\beta = V_{FD}/V_{OUT} = 1 - C_{fb}/C_{FD}$.

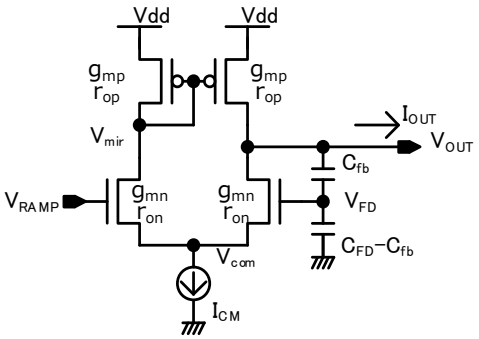

Figure 4: CM circuit and transistor parameters.

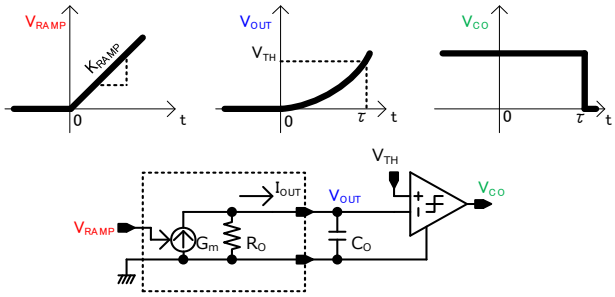

Figure 5: Equivalent circuit model of CM with output load capacitor Co and behavior of internal node signals.

In general, if the transimpedance of the CM is G_m and the output resistance is R_O, the relationship between the input and output currents of the CM is

$$\boldsymbol{I_{out}}=\boldsymbol{V_{RAMP}}\cdot\boldsymbol{G_m}-\boldsymbol{V_{out}}\frac{\boldsymbol{1}}{\boldsymbol{R_o}} \quad (2)$$

i.e., $\boldsymbol{G_m}=\boldsymbol{g_{mn}}\frac{\boldsymbol{1}}{\boldsymbol{R_o}}=\left(\frac{\boldsymbol{1}}{\boldsymbol{r_{on}}}+\frac{\boldsymbol{1}}{\boldsymbol{r_{op}}}+\boldsymbol{\beta}\cdot\boldsymbol{g_{mn}}\right)$.

The transconductance G_m is not affected by feedback factor of β.

B. Modeling of a MOS device operating in subthreshold region

In subthreshold current operation, a CMOS device is modeled using the Enz–Oguey mathematical approximation [18]. Following a previous study [12], we assumed the following circuit conditions under subthreshold current operation, ($\kappa(V_g - V_t) - V_s < 0$), and saturation, ($V_d - V_s \gg U_t$). Here, $U_t = kT/q$. The ratio of the reverse current to the forward current is assumed to be zero (i.e., $I_r/I_f \fallingdotseq 0$). Thus, we obtain

$$\boldsymbol{I_{ds}}=\boldsymbol{K_1}\cdot\exp\left\{\frac{\kappa(\boldsymbol{V_g}-\boldsymbol{V_t})}{\boldsymbol{U_t}}\right\}\cdot\exp\left(\frac{-\boldsymbol{V_s}}{\boldsymbol{U_t}}\right)\cdot(\boldsymbol{1}+\boldsymbol{\lambda}\cdot\boldsymbol{V_d}) \quad (3)$$

The MOS small-signal model parameter, G_m is obtained by differentiating Eqs. (3):

$$\boldsymbol{G_m}=\frac{\boldsymbol{d}\,\boldsymbol{I_{ds}}}{\boldsymbol{d}\,\boldsymbol{V_g}}$$

$$=\boldsymbol{K_1}\cdot\frac{\kappa}{\boldsymbol{U_t}}\cdot\exp\left\{\frac{\kappa(\boldsymbol{V_g}-\boldsymbol{V_t})}{\boldsymbol{U_t}}\right\}\cdot\exp\left(\frac{-\boldsymbol{V_s}}{\boldsymbol{U_t}}\right)\cdot(\boldsymbol{1}+\boldsymbol{\lambda}\cdot\boldsymbol{V_d})=\frac{\kappa}{\boldsymbol{U_t}}\cdot\boldsymbol{I_{ds}} \quad (4)$$

C. Noise bandwidth

When the CM includes an output load capacitor C_o (Figure 5), the output current is expressed by

$$\boldsymbol{I_{OUT}}(\boldsymbol{t})=\boldsymbol{C_O}\cdot\frac{\boldsymbol{d}}{\boldsymbol{dt}}\boldsymbol{V_{OUT}}(\boldsymbol{t})$$

From a general CM circuit expression,

$$\frac{d}{dt}V_{OUT}(t) + \omega_O \cdot V_{OUT}(t) = \frac{G_m}{C_O}V_{RAMP}$$

Here, $\omega_O = \frac{1}{R_O \cdot C_O}$. The solution under the following boundary condition,

$$V_{RAMP} = \begin{cases} 0, & t < 0 \\ K_{RAMP} \cdot t, & t \geq 0 \end{cases}$$

is

$$V_{OUT}(t) = \frac{G_m \cdot K_{RAMP}}{C_O \cdot \omega_O^2}\{\omega_O \cdot t - 1 + \exp(-\omega_O \cdot t)\} \quad (5)$$

Approximating Eq. (5) to the second-order terms of the Taylor–Maclaurin expansion, we obtain

$$V_{OUT}(t) \fallingdotseq \frac{G_m \cdot K_{RAMP}}{2C_O} \cdot t^2$$

In Figure 5, assuming that the output voltage reaches the CM threshold V_{TH} at time τ,

$$V_{TH} = \frac{G_m \cdot K_{RAMP}}{2C_O} \cdot \tau^2 \quad (6)$$

The noise bandwidth (NBW) of an ideal integrator under non wide-sense-stationary (WSS) conditions with window function from 0 to τ was previously reported [19][20]. We find that NBW=1 / 2τ and substituting Eq. (6), i.e.,

$$NBW = \frac{1}{2\tau} = \sqrt{\frac{G_m \cdot K_{RAMP}}{8C_O \cdot V_{TH}}} = \sqrt{\frac{\kappa_n \cdot I_{ds} \cdot K_{RAMP}}{kT/q \cdot 8C_O \cdot V_{TH}}} \quad (7)$$

D. Noise Power Spectral Density

In the case of the CM for the configuration shown in Figure 4, the PSD of the input-referred noise voltage is expressed by one-side frequency as follows:

$$PSD(f) = 4kT \cdot 2 \cdot \frac{\gamma_n}{g_{mn}}\left(1 + \frac{\gamma_p}{\gamma_n}\frac{g_{mp}}{g_{mn}}\right) \quad (8)$$

In subthreshold current operation, according to Eqs. (4), and substituting $g_{mn} = \frac{\kappa_n}{U_t} \cdot I_{ds}$ and $g_{mp} = \frac{\kappa_p}{U_t} \cdot I_{ds}$ into Eq. (8), we obtain:

$$PSD(f) = \frac{8(kT)^2 \cdot \gamma_n}{q \cdot \kappa_n \cdot I_{ds}}\left(1 + \frac{\gamma_p}{\gamma_n} \cdot \frac{\kappa_p}{\kappa_n}\right) \quad (9)$$

As we mentioned, no term exists in Eq. (9), depending on the W/L ratio.

E. Total Noise

For simplicity, the CDS function is approximated as $\sqrt{2}$, and the total input-referred thermal noise is obtained from Eq. (7) and Eq. (9).

$$\overline{v_{ni}^2} = 2 \cdot PSD \cdot NBW$$

$$= 2 \cdot \frac{8(kT)^2 \cdot \gamma_n}{q \cdot \kappa_n \cdot I_{ds}} \cdot \left(1 + \frac{\gamma_p}{\gamma_n} \cdot \frac{\kappa_p}{\kappa_n}\right) \cdot \left(\frac{\kappa_n \cdot I_{ds} \cdot K_{RAMP}}{kT/q \cdot 8C_O \cdot V_{TH}}\right)^{\frac{1}{2}}$$

$$v_{ni,rms} = 2^{\frac{5}{4}} \cdot (kT)^{\frac{3}{4}} \cdot \frac{\gamma_n^{\frac{1}{2}}}{(\kappa_n \cdot q)^{\frac{1}{4}}} \cdot \left(\frac{K_{RAMP}}{I_{ds} \cdot C_O \cdot V_{TH}}\right)^{\frac{1}{4}} \cdot \left(1 + \frac{\gamma_p}{\gamma_n} \cdot \frac{\kappa_p}{\kappa_n}\right)^{\frac{1}{2}} \quad (10)$$

From Eq. (10), the thermal noise of the single-slope ADC in subthreshold current operation is

--proportional to the 1/4 power of the DAC slope,

--inversely proportional to 1/4 of the power of I_{ds} (=I_{cm}/2) of the output load capacitor;

--the coupling feedback factor (β) from the output to the FD is not affected by the CM input referred noise,

--the transistor dimensions (W/L) do not affect the random noise,

from the circuit perspective. The remaining parameters affect the noise from a device perspective but are difficult to control significantly.

IV. Results

We confirmed the validity of Eq. (10), based on the measurement results from the prototype [11] and a transient noise simulation using the target device model parameters [21].

A. Measurement results of the prototype

Figure 6 shows the total RMS voltage noise versus the operating current I_{cm} for each DAC slope gain plotted on a double-logarithmic graph of the prototype [11]. The analog gains were 9064 V/s@ 0 dB, 4532 V/s@ 6 dB, and 2266 V/s@ 12 dB. The replotting shows that random noise is proportional to the power of 0.2, rather than 0.25 of I_{cm}. This result implies that the fitting parameters are necessary for Eq. (10), or the circuit model is too simplistic to account for noise.

B. Transient simulation results

We confirmed the design parameters in Eqs. (10) using transient noise simulation with fitted transistor parameters at I_{cm}=25 nA operation current for a 90 nm-pixel and 40 nm-logic process [21]. Figure 7 shows the circuit diagram, while Figure 8 shows the transient noise simulation results of the analog gain (K_{RAMP}) for each load capacitor.

The results show that the second-stage load capacitor is more effective than the first-stage capacitor when $K_{RAMP} \leqq$ 2266 V/s for this device model parameters. Although the noise-bandwidth suppression effect of the first-stage capacitor seems to disappear, the random noise is proportional to the power of 0.2 when a second-stage load capacitor of 10 fF is implemented. This means that the noise-bandwidth behavior varies between 9000 and 500 V/s K_{RAMP} and the 2nd stage noise becomes dominant. This noise behavior condition is not elucidated in this paper. It is clear that the scope of the noise analysis model should be expanded from a simple Gm-C-R 1st-stage equivalent circuit to the 2nd-stage of the comparator.

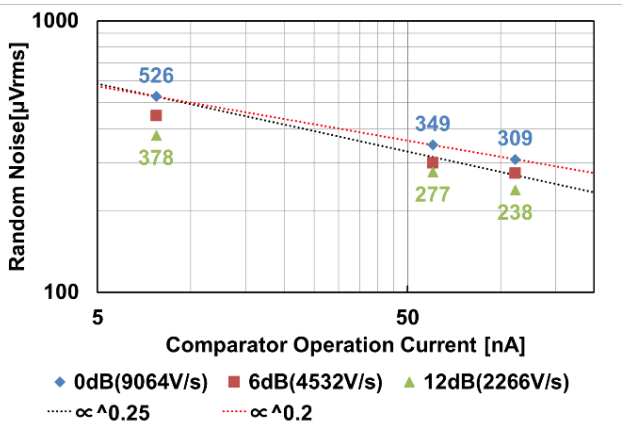

Figure 6: Random noise of the prototype [11] in double-logarithmic graph.

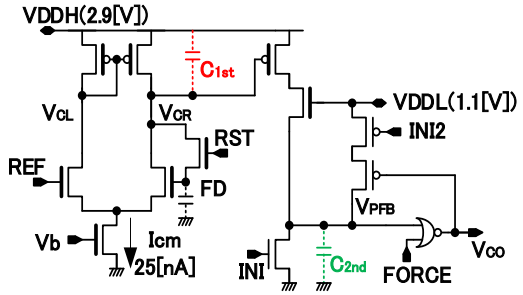

Figure 7: Simulation circuit for pixel-parallel ADC [21].

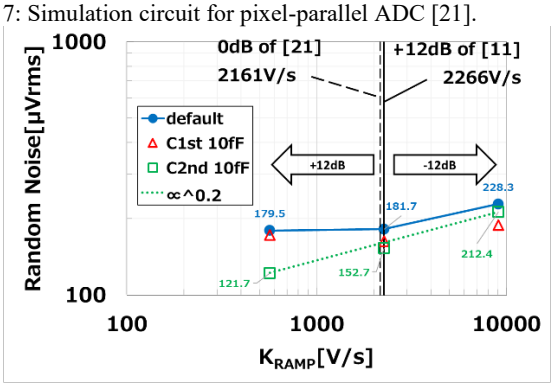

Figure 8: Random noise for load capacitor (C_{1st}, C_{2nd}) and DAC slope gain (K_{RAMP}) from transient random noise simulation.

V. Summary And Discussion

The comparator operation current I_{cm}, load capacitance, and slope of the DAC were derived as the noise-control parameters. From these investigations, we fabricated a sensor with I_{cm} = 25 nA, second-load capacitance of 13.8 fF implemented by a low-Vth NMOS (including a parasitic capacitance of 2.4 fF) within a 5.94 μm pixel-pitch, and K_{RAMP} = 2161 V/s@0 dB. This gain setting is approximately a +12 dB analog gain relative to the 0 dB of the prototype. Considering that the operation of the pixel-parallel A/D conversion operates once per frame, even if the A/D conversion time is increased owing to the +12 dB analog gain, the sensor frame rate is not significantly affected with respect to that of the column-parallel A/D conversion. The small 13.8 fF MOS capacitor of this device is more cost-effective than that reported in [14], where the band-limiting in-pixel capacitor was 100 fF. Furthermore, the absence of an in-pixel source follower and DC-cut sample-track capacitor results in further cost savings and noise reduction.

Finally, we realized a two-wafer stacked 25.2-Mpixel image sensor, including a pixel-parallel 14 bit ADC with a random noise of 167 μV_{rms}@0 dB, 120 fps operation, and power consumption of 1545 mW [21]. The conversion efficiency of this sensor is 62.7 μV/e-, i.e., 2.66 e^-_{rms} at 60 °C. The sensor achieves an FoM (e^-_{rms}·pJ/step) of 0.083, which is comparable to that of recently reported SOTA image sensors [5],[8].

The mode-change boundary condition of the random noise resulting from the equation describing the equivalent circuit and the variation in the coefficient from 0.25 to 0.2 remain open research questions. The measurement noise included quantization noise, 1/f and dark-current shot noise at 60 °C, but the equation proposed in this study does not consider it. We expect this study to serve as a basis for the future development of pixel-parallel ADC design strategies.

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